D.2 CPUID Feature Flags Related to Instruction Support

Only a subset of the CPUID feature flags provides information related to instruction support.

The feature flags related to supported instruction subsets are accessed via the *standard* function number 0000_0001h, the *extended* function number 8000_00001h, and the *structured extended* function number 0000_0007h.

The following table lists all flags related to instruction support. Entries for each flag provide the instruction or instruction subset corresponding to the flag, the CPUID function that must be executed to access the flag, and the bit position of the flag in the return value.The feature flags listed are used in Table D-2 on page 537:

Table D-1. Feature Flags for Instruction / Instruction Subset Support

Feature Flag	Instruction or Subset	CPUID Function[1]	Feature Flag Bit Position[2]
BASE	Base Instruction set	—	—
CLFSH	CLFLUSH	standard	EDX[19]
CMPXCHG8B	CMPXCHG8B	both	EDX[8]
CMPXCHG16B	CMPXCHG16B	standard	ECX[13]
CMOV	CMOV*cc*	both	EDX[15]
MSR	RDMSR / WRMSR	both	EDX[5]
TSC	RDTSC / RDTSCP	both	EDX[4]
RDTSCP	RDTSCP	extended	EDX[27]
SysCallSysRet	SYSCALL / SYSRET	extended	EDX[11]
SysEnterSysExit	SYSENTER / SYSEXIT	standard	EDX[11]
FPU	x87	both	EDX[0]
x87 && CMOV	FCMOV*cc*[3]	both	EDX[0] && EDX[15]
MMX	MMX	both	EDX[23]
3DNow	3DNow!	extended	EDX[31]
MmxExt	MMX Extensions	extended	EDX[22]
3DNowExt	3DNow! Extensions	extended	EDX[30]
3DNowPrefetch	PREFETCH / PREFETCHW	extended	ECX[8]
SSE	SSE1	standard	EDX[25]
SSE2	SSE2	standard	EDX[26]

Notes:

1. *standard* = Fn 0000_0001h; *extended* = Fn 8000_0001h; *both* means that both standard and extended CPUID functions return the same feature flag in the same bit position of the return value. For functions of the form xxxx_xxxx_x, the trailing digit is the value required in ECX.
2. Register and bit position of the return value that corresponds to the feature flag.
3. FCMOVcc instruction is supported if x87 and CMOVcc instructions are both supported.
4. XSAVE (and related) instructions require separate enablement.

Table D-1. Feature Flags for Instruction / Instruction Subset Support

Feature Flag	Instruction or Subset	CPUID Function[1]	Feature Flag Bit Position[2]
SSE3	SSE3	standard	ECX[0]
SSSE3	SSSE3	standard	ECX[9]
SSE4A	SSE4A	extended	ECX[6]
SSE41	SSE4.1	standard	ECX[19]
SSE42	SSE4.2	standard	ECX[20]
LM	Long Mode	extended	EDX[29]
SVM	Secure Virtual Machine	extended	ECX[2]
AVX	AVX	standard	ECX[28]
AVX2	AVX2	0000_0007_0	EBX[5]
XOP	XOP	extended	ECX[11]
AES	AES	standard	ECX[25]
FMA	FMA	standard	ECX[12]
FMA4	FMA4	extended	ECX[16]
F16C	16-bit floating-point conversion	standard	ECX[29]
RDRAND	RDRAND	standard	ECX[30]
ABM	LZCNT	extended	ECX[5]
BMI1	Bit Manipulation, group 1	0000_0007_0	EBX[3]
BMI2	Bit Manipulation, group 2	0000_0007_0	EBX[8]
POPCNT	POPCNT	standard	ECX[23]
TBM	Trailing bit manipulation	extended	ECX[21]
MOVBE	MOVBE	standard	ECX[22]
MONITOR	MONITOR / MWAIT	standard	ECX[3]
MONITORX	MONITORX / MWAITX	extended	ECX[29]
PCLMULQDQ	PCLMULQDQ	standard	ECX[1]
FXSR	FXSAVE / FXRSTOR	both	EDX[24]
SKINIT	SKINIT / STGI	extended	ECX[12]
LahfSahf	LAHF / SAHF	extended	ECX[0]
FSGSBASE	FS and GS base read and write	0000_0007_0	EBX[0]
SHA	SHA	0000_0007_0	EBX[29]
CLFLOPT	CLFLOPT	0000_0007_0	EBX[23]
SMAP	SMAP	0000_0007_0	EBX[20]
ADX	ADX	0000_0007_0	EBX[19]

Notes:

1. *standard* = Fn 0000_0001h; *extended* = Fn 8000_0001h; *both* means that both standard and extended CPUID functions return the same feature flag in the same bit position of the return value. For functions of the form xxxx_xxxx_x, the trailing digit is the value required in ECX.
2. Register and bit position of the return value that corresponds to the feature flag.
3. FCMOVcc instruction is supported if x87 and CMOVcc instructions are both supported.
4. XSAVE (and related) instructions require separate enablement.

Table D-1. Feature Flags for Instruction / Instruction Subset Support

Feature Flag	Instruction or Subset	CPUID Function[1]	Feature Flag Bit Position[2]
RDSEED	RDSEED	0000_0007_0	EBX[18]
SME	SME	8000_001F	EAX[0]
SEV	SEV	8000_001F	EAX[1]
PageFlushMsr	PageFlushMsr	8000_001F	EAX[2]
ES	ES	8000_001F	EAX[3]
CLZERO	CLZERO	8000_0008	EBX[0]
Instruction Retired Counter	Instruction Retired Counter	8000_0008	EBX[1]
Error Pointer Zero/Restore	Error Pointer Zero/Restore	8000_0008	EBX[2]
XSAVEOPT	XSAVEOPT	0000_000D_1	EAX[0]
XSAVEC	XSAVEC	0000_000D_1	EAX[1]
XGETBV w/ ECX=1	XGETBV w/ ECX=1	0000_000D_1	EAX[2]
XSAVES/XRSTORS	XSAVES/XRSTORS	0000_000D_1	EAX[3]
XSAVE	XSAVE / XRSTOR[4]	standard	ECX[26]

Notes:

1. *standard* = Fn 0000_0001h; *extended* = Fn 8000_0001h; *both* means that both standard and extended CPUID functions return the same feature flag in the same bit position of the return value. For functions of the form xxxx_xxxx_x, the trailing digit is the value required in ECX.
2. Register and bit position of the return value that corresponds to the feature flag.
3. FCMOVcc instruction is supported if x87 and CMOVcc instructions are both supported.
4. XSAVE (and related) instructions require separate enablement.

D.3 Instruction List

Table D-2 shows the minimum current privilege level (CPL) required to execute each instruction and the feature flag or flags that indicates support for that instruction. Each flag is listed in the column corresponding to the instruction group to which it belongs. Note that some instructions span groups.